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Amendments to the Claims:

Please cancel non-elected claims 12-18 as follows.

This listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of claims:

1. (Original) A media access controller comprising:

a local bus for connecting blocks of the media access controller with each other;

a CPU connected with the local bus to drive the media access controller;

a register unit connected with the local bus to store information used for software control of the CPU with respect to internal units of the media access controller;

a host interface unit connected with the local bus to manage an interface between the media access controller and a host;

a physical layer interface unit connected with the local bus to manage an interface between the media access controller and a physical layer;

a power-save master for generating a signal for requesting an occupation/occupation expiration of the local bus in response to a signal inputted via the local bus and a value of the register;

a bus arbiter for generating a signal controlling a use of the local bus in response to the signal generated from the power-save master;

a power control unit for generating signals determining whether to supply clocks and power to the respective blocks of the media access controller, in response to the control signal of the bus arbiter, the register values inputted via the local bus, and a power-save mode exiting signal provided from other blocks of the media access controller;

a phase-locked loop for generating clocks in response to the signal determining whether to supply the power, the signal being generated from the power control unit;

a clock generator receiving the phase-locked clock from the phase-locked loop to generate clocks required to the media access controller, and supplying or disabling the clocks generated according to the signal determining whether to supply the clock, the signal being generated from the power control unit; and

a wake-up timer for applying a power-save mode exiting signal to the power control unit in response to the signals inputted from the local bus and the clock generator.

2. (Original) The media access controller of claim 1, wherein a direct connection method is employed when supplying the power and clocks to respective processors of the media access controller according to the power-save mode exiting signal.

3. (Original) The media access controller of claim 1, wherein the register unit includes a clock disable register and a locktime register.

4. (Original) The media access controller of claim 3, wherein the locktime register stores a time required until an output of the phase-locked loop is settled.

5. (Original) The media access controller of claim 1, wherein the power control unit generates a plurality of state control signals PLL_PWDN, PLL_STA and CLK_EN for controlling the power and clocks of the media access controller, in response to a first control signal MST from the bus arbiter, a second control signal WKUP from the wake-up timer, a first input value VLOC from the locktime register, and a second input value VSTB from the clock disable register.

6. (Original) The media access controller of claim 5, wherein the power-save master generates one signal for requesting the occupation/occupation expiration of the bus, in response to the second input value VSTB from the clock disable register and the signal PLL_STA from the power control unit.

7. (Original) The media access controller of claim 6, wherein the power-save master is implemented with one register.

8. (Original) The media access controller of claim 1, wherein the power-save master generates one signal for requesting the occupation/occupation expiration of the bus, in response to the second input value VSTB from the clock disable register and the signal

PLL_STA from the power control unit.

9. (Original) The media access controller of claim 1, wherein the clock generator supplies or disables the clocks to the respective blocks of the media access controller in response to any one of the state control signals generated from the power control unit.

10. (Original) The media access controller of claim 1, wherein the wake-up timer includes a wake-up time register for storing a time DTIM and a wake-up count register for counting the time DTIM.

11. (Original) The media access controller of claim 9, wherein the wake-up timer copies the time DTIM of the wake-up time register into the wake-up count register in response to a control signal MST from the bus arbiter in the power-save mode, and counts a value of the wake-up time register in synchronization with a low-speed clock divided from the clock generator.

12. - 18. (Cancelled).